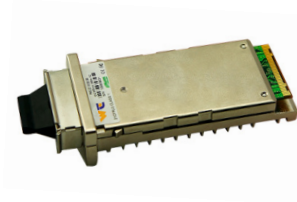


Product Specification

10Gb/s 1310nm Ethernet X2 Transceiver

☑ Features:

- Hot Z-pluggable
- XAUI Electrical Interface: 4lanse@3.125Gbit/s
- Below 4W power dissipation
- SC-Duplex Optical Receptacle
- Digital Diagnostic Monitor Interface
- Very low EMI and excellent ESD protection
- Uncooled 1310nm DFB laser and PIN ROSA
- Up to 10KM for single mode fiber
- Operating temperature range -40°C to 85°C



☑ Applications:

- 10G BASE-LR Ethernet
- Other optical links

☑ Standard:

- X2 MSA compliant
- IEEE802.3ae-2002 compliant
- GR-253-CORE compliant
- RoHS compliant

☑ Description:

WT's 10GbE X2 transceiver module WT-X2-LR is a hot pluggable in the Z-direction module that is usable in typical router line card applications, Storage, IP network and LAN and compliant to X2 MSA.

☑ Pin Definitions:

Pin #	Symbol	I/O	Logic	Description	Notes
1	GND	I	Supply	Electrical ground	
2	GND	I	Supply	Electrical ground	
3	GND	I	Supply	Electrical ground	
4	5.0 V	I	Supply	Power	
5	3.3 V	I	Supply	Power	
6	3.3 V	I	Supply	Power	
7	APS	I	Supply	Adaptive Power Supply	
8	APS	I	Supply	Adaptive Power Supply	
9	LASI	O	Open Drain	Link Alarm Status Interrupt. 10-22k ohm pull up on host.	
10	RESET	I	1.2V CMOS	TX OFF when MDIO RESET	
11	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
12	TX ON/OFF	I	1.2V CMOS	Transmitter ON/OFF	
13	RESERVED	-	-	Reserved	
14	MOD DETECT	O	-	Pulled low inside module through 1k ohm.	
15	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	

☑ Pin Definitions:

Pin #	Symbol	I/O	Logic	Description	Notes
16	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
17	MDIO	I/O	Open Drain	Management Data IO	
18	MDC	I	1.2V CMOS	Management Data Clock	
19	PRTAD4	I	1.2V CMOS	Port Address bit 4 (Low=0)	
20	PRTAD3	I	1.2V CMOS	Port Address bit 3 (Low=0)	
21	PRTAD2	I	1.2V CMOS	Port Address bit 2 (Low=0)	
22	PRTAD1	I	1.2V CMOS	Port Address bit 1 (Low=0)	
23	PRTAD0	I	1.2V CMOS	Port Address bit 0 (Low=0)	
24	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
25	APS SET	O	-	Feedback output for APS	
26	RESERVED	-	-	Reserved for Avalanche Photodiode use.	
27	APS SENSE	O	Analog	APS Sense Connection	
28	APS	I	Supply	Adaptive Power Supply	
29	APS	I	Supply	Adaptive Power Supply	
30	3.3 V	I	Supply	Power	
31	3.3 V	I	Supply	Power	
32	5.0 V	I	Supply	Power	
33	GND	I	Supply	Electrical Ground	
34	GND	I	Supply	Electrical Ground	
35	GND	I	Supply	Electrical Ground	

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☑ Pin Definitions:

Pin #	Symbol	I/O	Logic	Description	Notes
36	GND	I	Supply	Electrical Ground	
37	GND	I	Supply	Electrical Ground	
38	RESERVED	-	-	Reserved	
39	RESERVED	-	-	Reserved	
40	GND	I	Supply	Electrical Ground	
41	RX LANE 0+	O	AC	Module XAUI Output Lane 0+	
42	RX LANE 0-	O	AC	Module XAUI Output Lane 0-	
43	GND	I	Supply	Electrical Ground	
44	RX LANE 1+	O	AC	Module XAUI Output Lane 1+	
45	RX LANE 1-	O	AC	Module XAUI Output Lane 1-	
46	GND	I	Supply	Electrical Ground	
47	RX LANE 2+	O	AC	Module XAUI Output Lane 2+	
48	RX LANE 2-	O	AC	Module XAUI Output Lane 2-	
49	GND	I	Supply	Electrical Ground	
50	RX LANE 3+	O	AC	Module XAUI Output Lane 3+	
51	RX LANE 3-	O	AC	Module XAUI Output Lane 3-	
52	GND	I	Supply	Electrical Ground	
53	GND	I	Supply	Electrical Ground	
54	GND	I	Supply	Electrical Ground	
55	TX LANE 0+	I	AC	Module XAUI Input Lane 0+	
56	TX LANE 0-	I	AC	Module XAUI Input Lane 0-	
57	GND	I	Supply	Electrical Ground	
58	TX LANE 1+	I	AC	Module XAUI Input Lane 1+	
59	TX LANE 1-	I	AC	Module XAUI Input Lane 1-	
60	GND	I	Supply	Electrical Ground	
61	TX LANE 2+	I	AC	Module XAUI Input Lane 2+	
62	TX LANE 2-	I	AC	Module XAUI Input Lane 2-	
63	GND	I	Supply	Electrical Ground	
64	TX LANE 3+	I	AC	Module XAUI Input Lane 3+	
65	TX LANE 3-	I	AC	Module XAUI Input Lane 3-	
66	GND	I	Supply	Electrical Ground	
67	RESERVED	-	-	Reserved	
68	RESERVED	-	-	Reserved	
69	GND	I	Supply	Electrical Ground	
70	GND	I	Supply	Electrical Ground	

70	GND	1	GND
69	GND	2	GND
68	RESERVED	3	GND
67	RESERVED	4	5.0V
66	GND	5	3.3V
65	TX LANE3-	6	3.3V
64	TX LANE3+	7	APS
63	GND	8	APS
62	TX LANE2-	9	LASI
61	TX LANE2+	10	RESET
60	GND	11	VEND SPECIFIC
59	TX LANE1-	12	TX ON/OFF
58	TX LANE1+	13	RESERVED
57	GND	14	MOD DETECT
56	TX LANE0-	15	VEND SPECIFIC
55	TX LANE0+	16	VEND SPECIFIC
54	GND	17	MDIO
53	GND	18	MDC
52	GND	19	PRTAD4
51	RX LANE3-	20	PRTAD3
50	RX LANE3+	21	PRTAD2
49	GND	22	PRTAD1
48	RX LANE2-	23	PRTAD0
47	RX LANE2+	24	VEND SPECIFIC
46	GND	25	APS SET
45	RX LANE1-	26	RESERVED
44	RX LANE1+	27	APS SENSE
43	GND	28	APS
42	RX LANE0-	29	APS
41	RX LANE0+	30	3.3V
40	GND	31	3.3V
39	RESERVED	32	5.0V
38	RESERVED	33	GND
37	GND	34	GND
36	GND	35	GND

Transceiver PCB Bottom of Transceiver PCB
(as viewed through top)

Absolute Maximum

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	TS	-40	85	°C
Case Temperature	Tc	0	70	°C
Power Supply Voltage	VCC3	0	4.0	V
	Vcc5	0	5.5	V
	Vccaps	0	1.5	V
Operating Relative Humidity	RH		85	%

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☑ Electrical Characteristics:

Transmitter(-40~85 °C @9.953Gb/s~11.1Gb/s)						
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Date Rate			10.3125		Gb/s	
Ave. Output Power	Po		-2		dBm	1
Output Centre Wavelength	λ	1260		1350	nm	
Disable Power	Poff			-30	dBm	
Extinction Ratio	ER	3.5			dB	1
Sidemode Supression Ratio		30			dB	
Rise/Fall Time (20%~80%)	Tr/Tf			45	ps	
Signal Speed Variation from nominal		-100		100	ppm	

Receiver(-40~85 °C @9.953Gb/s~11.1Gb/s)							
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note	
Operating Date Rate			10.312		Gb/s		
Overload	Po	0.5			dBm		
Input Centre Wavelength	λ	1260		1350	nm		
Receiver Sensitivity	Pmin			-14.4	dBm	1	
Stressed Sensitivity in OMA				-11.3	dBm	2	
LOS Assert	LosA	-30			dBm		
LOS De-assert	LosD			-18	dBm		
LOS Hysteresis		0.5		4	dB		
Optical Return Loss		14			dB		
Jitter Tolerance		GR-253-CORE/ITU-T G.783					1

Note :

1. Measured at 9.95328Gb/s,Framed PRBS2^31-1,NRZ
2. Measured at 10.3125Gb/s,Non-framed PRBS2^31-1,NRZ

☑ MDIO Operation:

Frame	Management frame fields							IDLE
	PRE	ST	OP	PRTAD	DEVAD	TA	ADDRESS/DATA	
Address	1...1	00	00	PPPPP	EEEEEE	10	AAAAAAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	EEEEEE	10	DDDDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	EEEEEE	Z0	DDDDDDDDDDDDDDDDDD	Z
Read.inc	1...1	00	10	PPPPP	EEEEEE	Z0	DDDDDDDDDDDDDDDDDD	Z

PRE = Preamble, Which consists of 32bit '1's

ST = Start of Frame indicated by 00 pattern

OP = Access Type

- '00' for Address
- '01' for Write
- '11' for Read
- '10' for Post Read Incremented Address

TA = Turnaround: Z0 for Read, and '10' for Write

PRTAD = Physical Address(hardwired)

DEVAD = Device Type

- '00000' for Reserved
- '00001' for PMA/PMD or User-defined Register(including NVR memory)
- '00010' for WIS(Not implemented)
- '00011' for PCS or X2 Register(including NVR memory)
- '00100' for PHY XS or X2 Register(including NVR memory)
- '00101' for DTE XS(Not implemented)

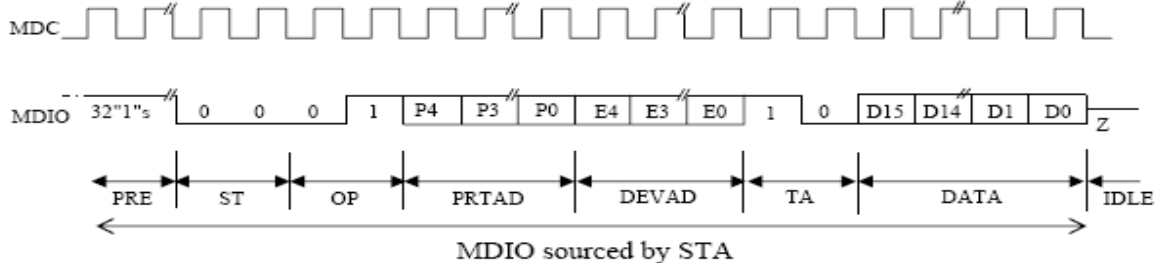


Figure 21 MDIO/MDC Timing Diagram during the Write/Address Operation

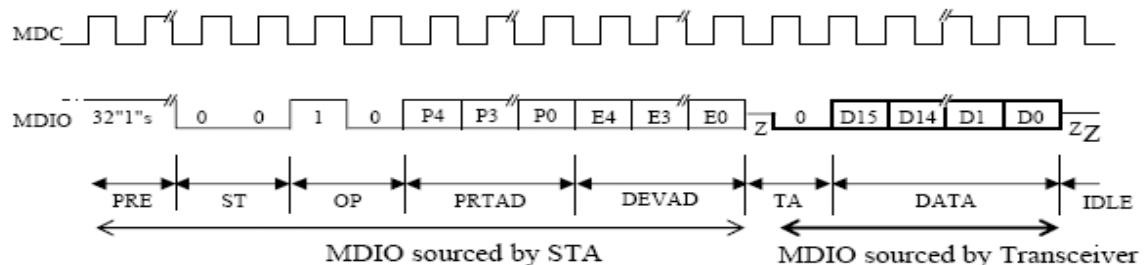
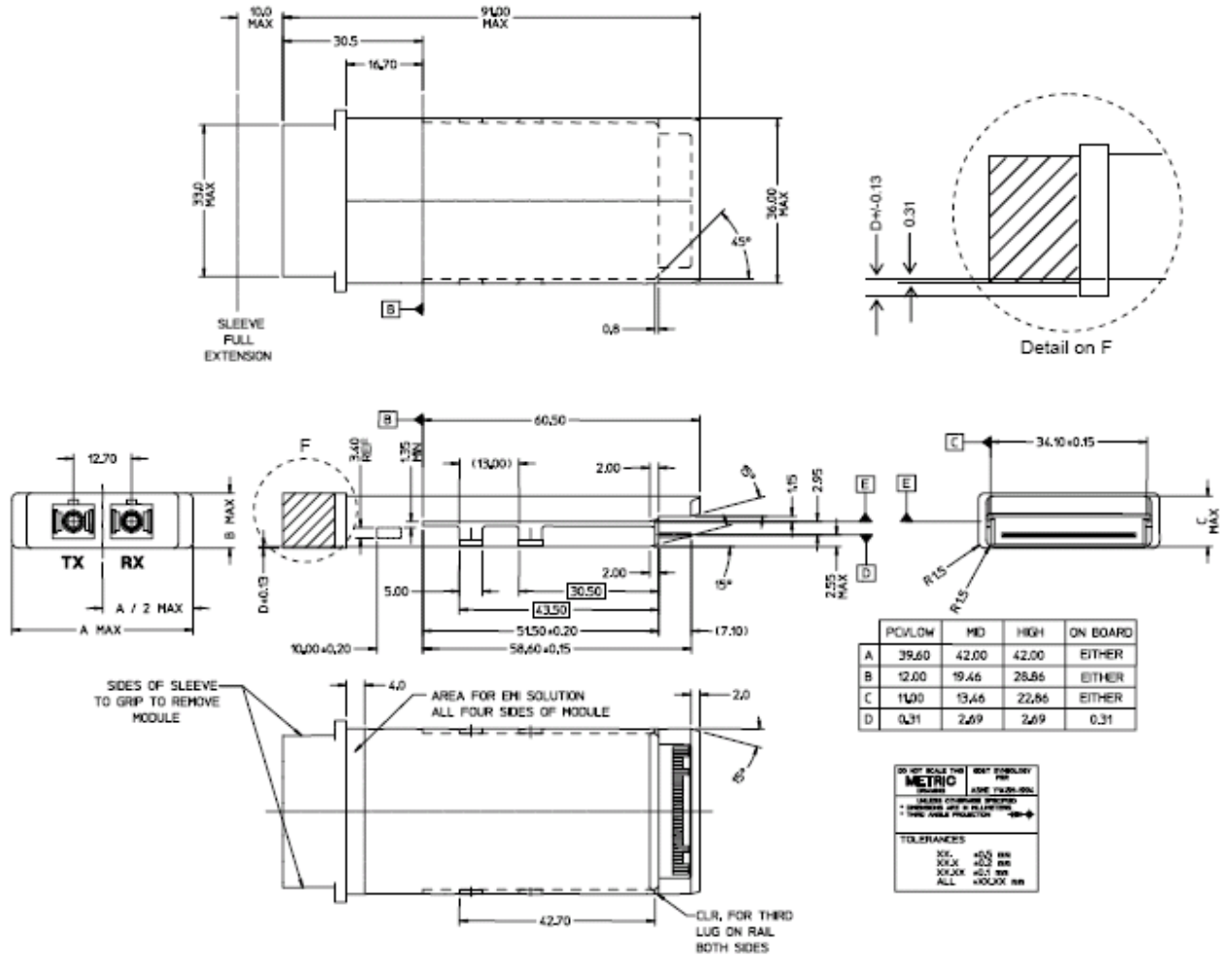


Figure 22 MDIO/MDC Timing Diagram during the Read/Read inc Operation

Package Dimensions:



Package Dimensions:

